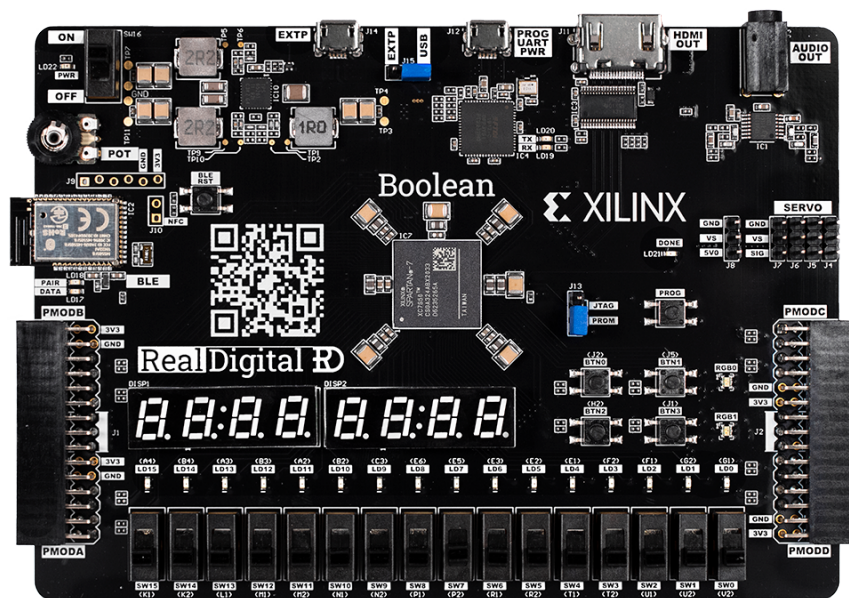


Digital Electronics – Lab 1

Truth Table

Kent Abrahamsson, Andreas Lönn

2026-01-18



Revision history

Date	Author	Description
2023-03-27	Kent Abrahamsson	First edition
2023-04-01	Kent Abrahamsson	Minor typo fix
2026-01-18	Andreas Lönn	From Altera to Xilinx

Contents

1	General	4
1.1	Background	4
1.2	Intended outcome	4
1.3	Checkpoints	4
2	Lab instructions	5
2.1	General	5
2.2	Design method 1	6
2.3	Design method 2	6
2.4	Design method X (not mandatory)	6

1 General

1.1 Background

This document is intended to be used as Lab instructions for the Truth Table lab in the VHDL course.

1.2 Intended outcome

Truth table functionality shall be implemented using at least two different methods.

1.3 Checkpoints

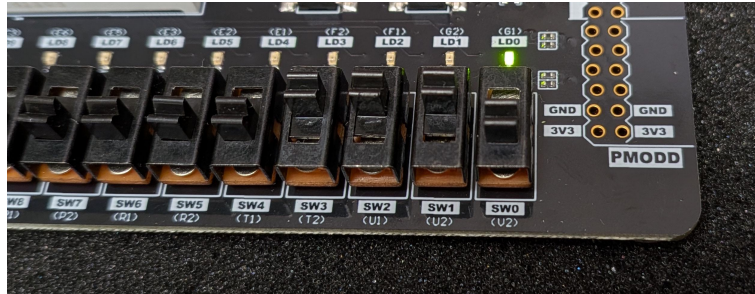
In order to Pass the lab assignment the student shall be able to show that the following tasks have been fulfilled. Consult Lab 0 if you have questions.

- Two different Vivado projects have been created. Each project shall be stored in its own project folder.
- Properly written VHDL implementation for in both projects. Use proper indentation; spaces are cheap!
- Student have understood how pins in the constraints file are mapped to the signal names in the design entity.
- A simulation for one of the methods shall be shown.
- RTL Analysis for both methods shall be performed to compare the schematics.
- The two methods shall have been run on the FPGA board.

2 Lab instructions

2.1 General

In this assignment you shall implement simple asynchronous logic to realize the functionality specified in a truth table. You will use 8 of the slide switches on the development board as inputs, and one LED as output.



The 16 rocker switches in the row are connected to different I/O-pins on the FPGA. The pin number for each switch is found in the schematic or user manual for the development board. The reference manual and schematics of the Boolean board can be found on RealDigital's website.

In the constraints file that you received for this lab, all ports have been commented out. Uncomment (remove the '#' at the start of the line) all ports that you need for the lab.

The development board also have a number of LEDs that can be used as generic outputs. Use one of the LEDs (e.g. LD0) as output for your design in this lab.

The following truth table shall be implemented:

SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	LED output
0	0	0	0	0	0	0	1	ON
0	0	0	0	0	0	1	1	ON
0	0	0	0	0	1	1	1	ON
0	0	0	0	1	1	1	0	ON
0	0	0	1	1	1	0	0	ON
0	0	1	1	1	0	0	0	ON
0	1	1	1	0	0	0	0	ON
1	1	1	0	0	0	0	0	ON

All other combinations (not shown above) shall keep LED output switched OFF.

2.2 Design method 1

Accept the invitation to the assignment on GitHub Classroom (see Canvas), clone the repository, and create the project in the `Lab1_Method_1` directory using the Tcl script (see Lab 0). Add all signals for the LED and switches in the entity.

Implement the functionality using only Boolean expressions (and / or / not).

2.3 Design method 2

Create the project in the `Lab1_Method_2` directory using the Tcl script. Add all signals for the LED and switches in the entity.

Implement the functionality using a single process and if / elsif / else statements.

2.4 Design method X (not mandatory)

Create the project in the `Lab1_Method_X` directory using the Tcl script. Add all signals for the LED and switches in the entity.

Add an additional LED output e.g. LD1 and implement both methods in the same file, each method driving its own unique LED.